

8A, 200V, 0.600 Ohm, Logic Level, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V to 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

Formerly developmental type TA09534.

Ordering Information

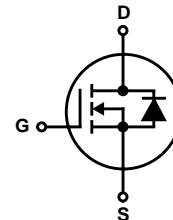
PART NUMBER	PACKAGE	BRAND
RFP8N20L	TO-220AB	RFP8N20L

NOTE: When ordering, include the entire part number.

Features

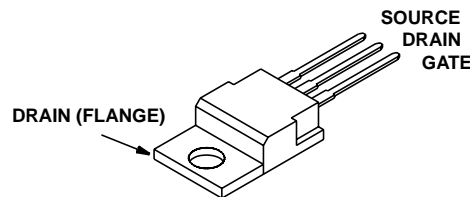
- 8A, 200V
- $r_{DS(ON)} = 0.600\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedence
- Majority Carrier Device
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-220AB



RFP8N20L

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	RFP8N20L	UNITS
Drain to Source Voltage (Note 1)	200	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	200	V
Continuous Drain Current	8	A
Pulsed Drain Current (Note 3)	20	A
Gate to Source Voltage	10	V
Maximum Power Dissipation	60	W
Above $T_C = 25^\circ\text{C}$, Derate Linearly	0.48	$\text{W}/^\circ\text{C}$
Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	200	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ $T_C = 25^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ $T_C = 125^\circ\text{C}$	-	-	50	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = 10\text{V}$, $V_{DS} = 0$	-	-	100	nA
Drain to Source On-Voltage (Note 2)	$V_{DS(ON)}$	$I_D = 8\text{A}$, $V_{GS} = 5\text{V}$	-	-	4.8	V
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 4\text{A}$, $V_{GS} = 5\text{V}$	-	-	0.600	Ω
Turn On Delay Time	$t_{d(ON)}$	$I_D = 4\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 6.25$, $V_{GS} = 5\text{V}$	-	15	45	ns
Rise Time	t_r		-	45	150	ns
Turn Off Delay Time	$t_{d(OFF)}$		-	100	135	ns
Fall Time	t_f		-	60	105	ns
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$	-	-	900	pF
Output Capacitance	C_{OSS}		-	-	250	pF
Reverse Transfer Capacitance	C_{RSS}		-	-	120	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	RFP8N20L			2.083	$^\circ\text{C}/\text{W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = 4\text{A}$	-	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = 4\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	250	-	ns

NOTES:

2. Pulsed: pulse duration = $300\mu\text{s}$ max, duty cycle = 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

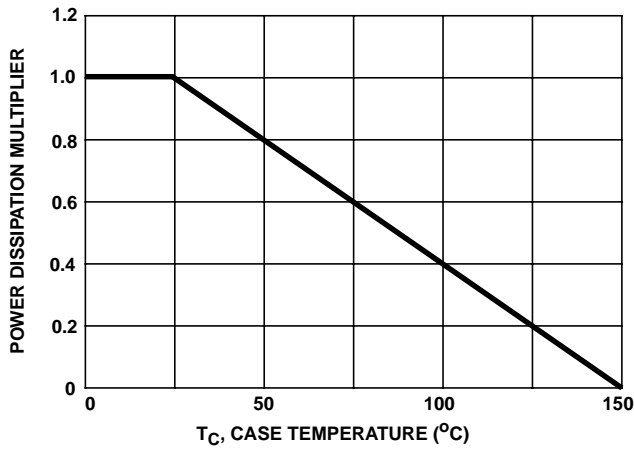


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

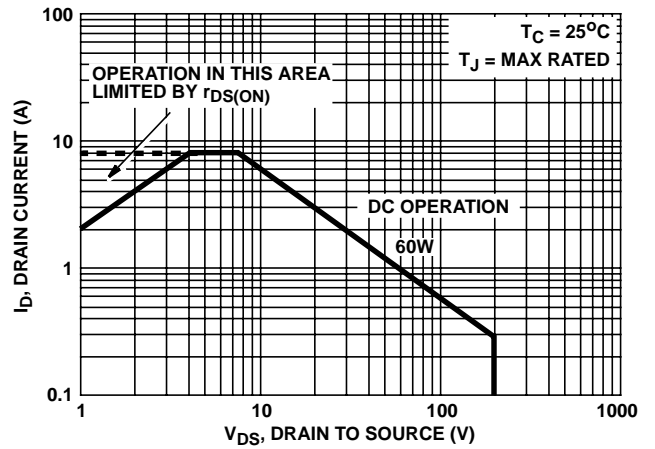


FIGURE 2. FORWARD BIAS SAFE OPERATING AREA

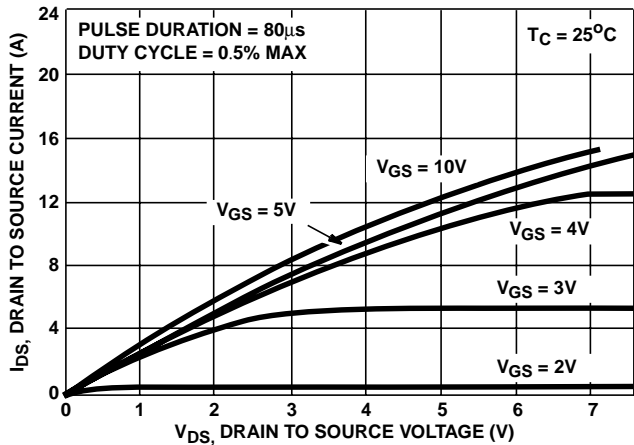


FIGURE 3. SATURATION CHARACTERISTICS

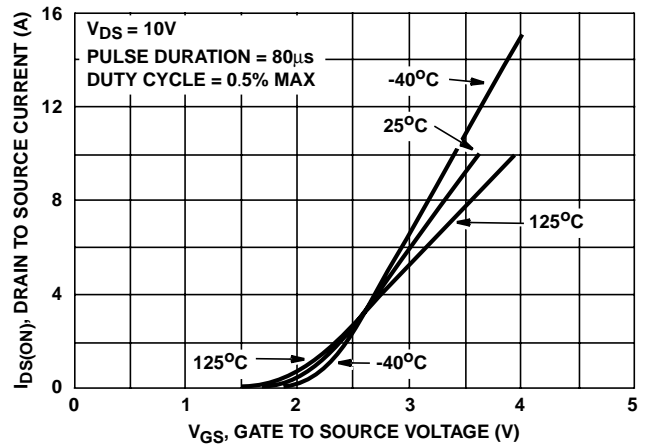


FIGURE 4. TRANSFER CHARACTERISTICS

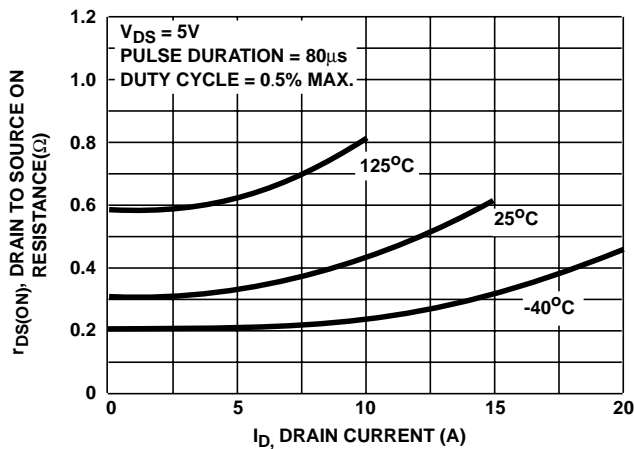


FIGURE 5. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

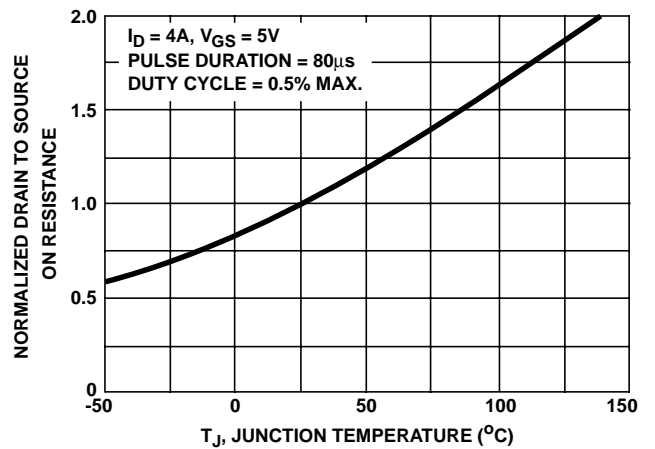


FIGURE 6. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

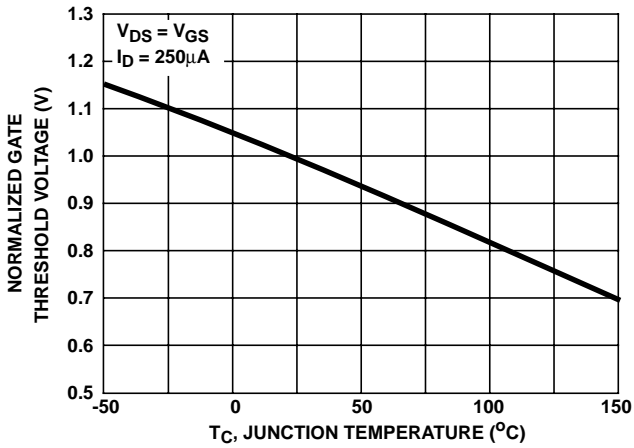


FIGURE 7. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

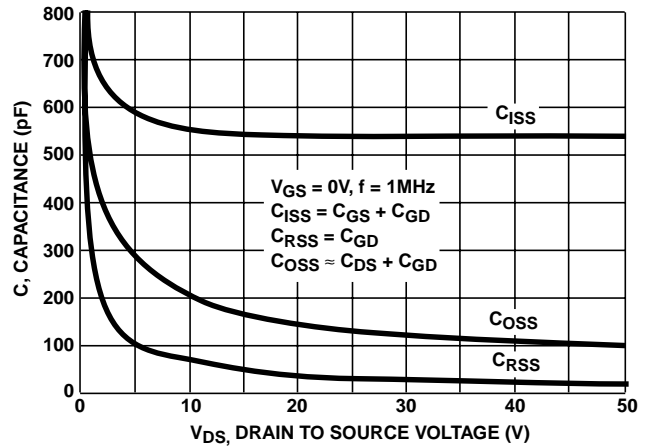
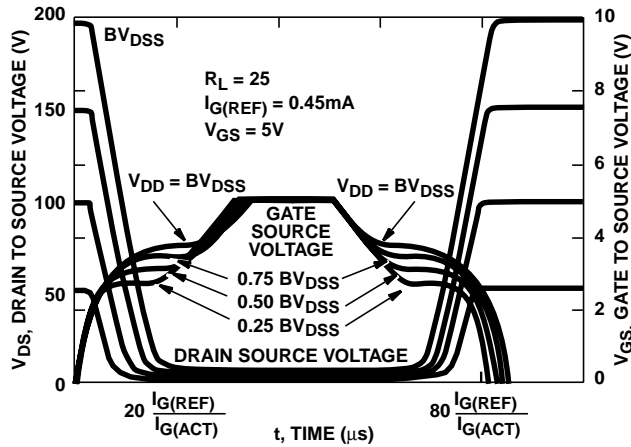


FIGURE 8. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 9. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

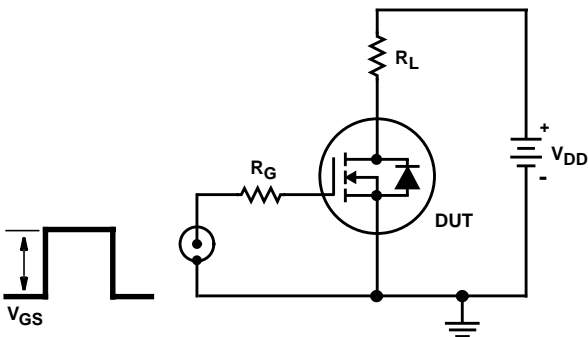


FIGURE 10. SWITCHING TIME TEST CIRCUIT

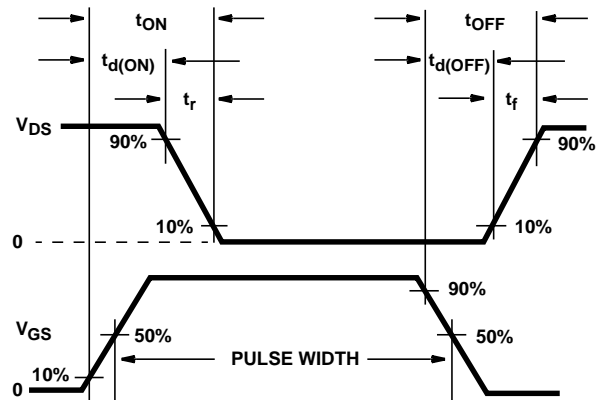


FIGURE 11. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

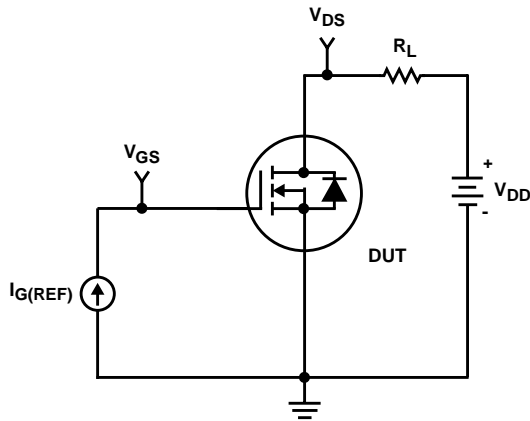


FIGURE 12. GATE CHARGE TEST CIRCUIT

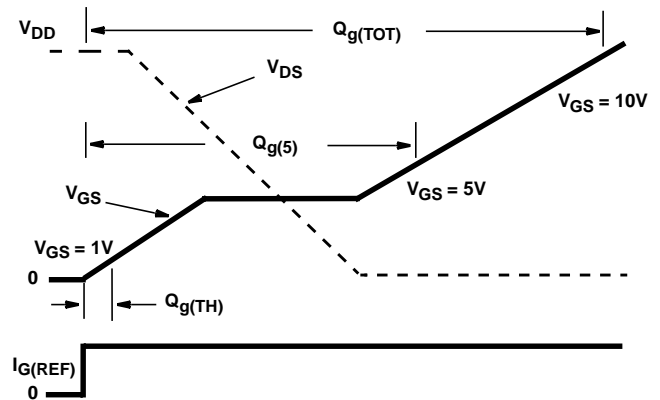


FIGURE 13. GATE CHARGE WAVEFORMS

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